(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

THIRD SEMESTER [BCA] DECEMBER 2025-JANUARY 2026

Paper Code: BCA205T **Subject: Computer Organization & Architecture**

(BATCH 2024)

Time: 3 Hours **Maximum Marks: 60**

Note: Attempt all questions as directed. Internal choice is indicated.

Q1 Attempt **any Four** of the following questions: **(4x5 =20)**

(a) Explain the concept of micro-operations with an example.
(b) State the purpose of control functions in register transfer language (RTL).
(c) Design the logic circuit for $Y = (A + B)' + C$ using NAND gates.
(d) Convert the expression $F = A'BC + AB'C + ABC'$ into canonical SOP form.
(e) Write the SOP and POS forms for the truth table where $F(A,B,C)$= 1 for minterms (1,3,5,7).
(f) Draw a 4-bit synchronous up/down counter.
(g) Give the symbolic description for the reference instructions: BUN, SKI, STA, BSA and ISZ?
(h) What do you mean by level-triggered and edge-triggered circuits?

Q2 (a) Simplify the following Boolean function for 4-variable F(A,B, C, D)=Σ(0,1,2,5,8,9,10,14). Draw logic gate only using basic gates. **(5)**

(b) Convert the expression $F = A'BC + AB'C + ABC'$ into canonical SOP form. **(5)**

OR

Q3 (a) Design and explain the working of a JK flip-flop using NAND gates. **(5)**
(b) Design a 4-bit binary counter using T flip-flops and explain its working. **(5)**

Q4 (a) Draw and explain the block diagram of a 4-bit Register with Parallel Load Capability. **(5)**
(b) Draw and explain the block diagram of CPU registers and bus structure. **(5)**

OR

Q5 (a) Explain the memory transfer operations and show how read and write operations are executed using registers and control signals. **(5)**
(b) Explain the different data transfer modes in computer systems. **(5)**

Q6 (a) What is Instruction Format? Draw and explain the flowchart of Instruction Cycle. **(5)**
(b) Discuss various types of addressing modes with suitable examples. **(5)**

OR

Q7 (a) Explain I/O mapped I/O and memory-mapped I/O with differences. **(5)**
(b) What is bus arbitration? Describe daisy chaining and parallel priority interrupt methods. **(5)**

Q8 (a) What is virtual memory? Explain its working with the help of a suitable diagram **(5)**
(b) Describe the concept of cache mapping techniques: Direct, Associative, and Set-Associative Mapping. **(5)**

OR

Q9. (a) Draw and explain the block diagram of a DMA controller. **(5)**
(b) Describe the working of DMA during a data transfer operation. **(5)**

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